REDUCED POWER REGISTERED MEMORY MODULE AND METHOD

TECHNICAL FIELD

The invention relates to dynamic random access memory devices, and, more particularly, to a method and system for reducing the power consumed by registered memory modules.

BACKGROUND OF THE INVENTION

Dynamic random access memory ("DRAM") devices are commonly used in a wide variety of applications. One of the most common use for DRAM devices is as system memory in personal computers. The speed and capacity demands on DRAM devices continues to increase in this and other applications. However, power is consumed each time a digital circuit is switched to change the state of a signal line. The rate at which power is consumed by DRAM devices therefore increases with both the capacity and the operating speed of the devices. Thus, the demands for ever increasing memory capacities and speeds are inconsistent with the demands for ever decreasing memory power consumption.

For many applications, it is particularly important to limit the power consumption of DRAM devices. For example, DRAM devices used as system memory in portable personal computers should consume relatively little power to allow a battery to power the computer over an extended period. The limited period over which electronic devices, such as portable computers, can operated has been addressed by both attempts to increase battery life and attempts to reduce the rate at which such devices consume power. Excessive power consumption can also create problems even where DRAM devices are not powered by batteries. For example, the heat generated by excessive power consumption can damage the DRAM devices, and it can be difficult and/or expensive to maintain the temperature of electronic equipment containing the DRAM devices at an acceptably low value.

Various techniques have been used to reduce power consumption in electronic equipment containing DRAM devices. One approach has been to prevent

digital circuits from switching when such circuits are not active since, as mentioned above, power is consumed each time a component in the digital circuit is switched from one state to another. While this approach can significantly reduce the power consumed by DRAM devices, there are circuits in DRAM devices that cannot be rendered inactive without compromising the speed and/or operability of the DRAM devices. For example, a computer system may use several registered DRAM modules 10a-c as shown in Figure 1. Each module 10 includes two DRAM devices 12, 14, although a greater number of DRAM devices may be included in registered DRAM modules. The DRAM modules 10 also include a register 20 that receives control signals coupled through a control bus 24 and address signals coupled through an address bus 26. These control and address signals are latched in the register 20 responsive to an internal clock ICLK signal. The ICLK signal is generated by a phase-lock loop 34 from an external clock ("CKO") signal, which is applied to the modules 10 though a clock line 35. In one commercially available registered DRAM module, these control signals that are applied to the register include a row address strobe signal ("RAS#") (the "#" indicates the signal is active low), a column address strobe signal ("CAS#"), clock enable signals ("CKE0" and "CKE1"), a write enable signal ("WE#") and chip select signals ("S0#" and "S1#") to activate the DRAM devices 12, 14, respectively. Other signals not latched by the register 20 include the clock CK0 signal, data signals ("DQ0-DQ63") corresponding to a 64-bit data word applied to the modules through a data bus 28, and a number of other signals that are not pertinent to the present discussion. In this commercially available registered DRAM module, bank address signals ("B0-B1") corresponding to a 2-bit bank address and row/column address signals ("A0-A12") corresponding to a 13-bit address are also applied to the register 20 through the address bus 26.

The register 20 used in the registered DRAM modules 10a-c of Figure 1 is shown in Figure 2. Each of the control and address signals that are applied to the register 20 are applied to the data input of a respective flip-flop 30. The flip-flops 30 are clocked by an internal clock signal ICLK generated at the output of a phase-lock loop 34. The phase-lock loop 34 receives the clock signal CK0 so that the phase of the

internal clock signal ICLK matches the phase of the externally applied clock signal CK0. The use of the phase-lock loop 34 to generate the internal clock signal ICLK avoid excessive loading of the external clock signal CK0 since the clock signal must be applied to a number of circuits in each module 10. The signals applied to the flip-flops 30 are latched on each rising edge of the internal clock signals ICLK.

Returning to Figure 1, in operation, address signals A0-A12 and the previously mentioned control signals are simultaneously applied to all of the registered DRAM modules 10a-c, and all of these signals are latched into the registers 20 in all of these modules 10a-c. Each module 10a-c receives a different pair of chip select signals that designates which of the modules 10a-c is being accessed. Latching a large number of signals into the flip-flops 30 in each of the several modules 10a-c on each edge of a high speed clock signal can consume a significant amount of power since, as previously mentioned, power is consumed each time a digital circuit switches state. However, only one of the modules 10a-c is selected for a memory access by switching its chip select signals S0# and S1# active low. Therefore, the power consumed by the modules 10a-c that are not being selected for the memory access is unnecessarily consumed. This unnecessary power consumption can be significant since a large number of signals are latched into the registers 20 of each of the inactive modules 10 on each rising edge of the clock signal CLK0, which may have a frequency of 133 mHz or higher.

There is therefore a need for a method and system to prevent power from being needlessly consumed by registered DRAM modules.

SUMMARY OF THE INVENTION

A registered memory module and method includes a register receiving a plurality of signals at respective input terminals. The register stores the input signals responsive to a transition of an internal clock signal applied to a clock terminal of the register when an enable signal is active. The registered memory module also includes a plurality of memory devices coupled to output terminals of the register. Each of the memory devices is selected by a respective select signal being active. A logic circuit in the module receives the select signals for the memory devices and determines if any of

the select signals is active indicative of an access to a memory device in the module. If any of the select signals is active, the logic circuit applies an active enable signal to the register. If none of the select signals is active, the logic circuit applies an inactive enable signal to the register. As a result, if a memory access is not directed to a memory device in the module, the register in the module does not consume a significant amount of power by storing signals responsive to transitions of the internal clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a portion of a conventional computer system containing several commercially available registered DRAM modules.

Figure 2 is a logic diagram of a register used in the conventional registered DRAM module of Figure 2.

Figure 3 is a block diagram of a computer system containing several registered DRAM modules according to one embodiment of the invention.

Figure 4 is a logic diagram of one embodiment of a register used in the registered DRAM module of Figure 2.

Figure 5 is a logic diagram of another embodiment of a register used in the registered DRAM module of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

A computer system 40 containing two registered DRAM modules 44, 46 in accordance with one embodiment of the invention is shown in Figure 3. The computer system 40 includes a processor 60 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 60 is coupled to a processor bus 64 that normally includes an address bus, a control bus, and a data bus. In addition, the computer system 40 includes one or more input devices 66, such as a keyboard or a mouse, coupled to the processor 60 through a system controller 68 to allow an operator to interface with the computer system 40. Typically, the computer system 40 also includes one or more output devices 70 coupled to the processor 60 through the system controller 68, such output devices

typically being a printer or a video terminal. One or more data storage devices 74 are also typically coupled to the processor 60 through the system controller 68 to allow the processor 60 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 74 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). The processor 60 is also typically coupled to cache memory 78, which is usually static random access memory ("SRAM"). The system controller 68 also includes a memory controller 80 that is coupled to both of the registered DRAM modules 44, 46 through an address bus 84, a control bus 86 and a data bus 88. Each of the DRAM modules 44, 46 includes four synchronous DRAM ("SDRAM") devices 90, 92, 94, 96 as well as a register 100 and a phase-lock loop ("PLL") 104. Each of the SDRAM devices 90-96 is selected by a respective chip select signal CS0#, CS1#, CS2#, CS3#, all of which are coupled to the registers 100 in the modules 44, 46 through the control bus 86. The control bus 86 also couples a clock enable signal CKE to the SDRAMs 90-96 in the modules 44, 46, and a clock signal CLK to the PLLs 104 in the modules 44, 46. The PLLs 104 generate an internal clock signal ICLK that is synchronized to the externally applied clock signal CLK. The CKE signal is applied to the SDRAM devices 90-96 in the modules 44, 46 through the registers 100. In other types of registered memory modules, such as modules using double data rate ("DDR") DRAMs, it may be necessary for other signals to be applied directly to memory devices in the modules.

One embodiment of a register 108 that may be used for the registers 100 in the modules 44, 46 is shown in Figure 4. The register 108 includes a flip-flop 110 for each of the signals that is applied to the register 100. Each flip-flop 110 includes a data "D" input to which the externally applied signal is coupled, a clock input "C" to which the ICLK signal is coupled, and a clock enable "CE" input that receives an enable signal. The enable signal applied to the CE input allow the ICLK signal to latch the signal applied to the D input on a transition, such as the rising edge, of the ICLK signal. The enable signal applied to the CE input is generated by a NAND gate 114 having four inputs that receive the four chip select signals CS0#-CS3#. As mentioned above, the chip select signals CS0#-CS3# are active low. As a result, the output of the NAND gate

114 will be high to enable the flip-flops 110 if any of the chip select signals CS0#-CS3# is active low. Thus, the register 100 in one of the modules 44, 46 will latch the signals applied to its inputs responsive to the ICLK signal if any of the SDRAMs 90-96 in the module 44, 46 is selected by the memory controller 80. Significantly, however, if none of the chip select signals CS0#-CS3# is active low, all of the inputs to the NAND gate 114 will be high, thereby causing the NAND gate 114 to apply a low to the CE inputs of the flip-flops 110. As a result, the flip-flops 110 will not latch the signals applied to their D inputs responsive to the CLK signal. By causing the registers 100 to refrain from responding to the CLK signal if none of the SDRAMs 90-96 in the module 44, 46 is selected, the non-enabled register 44, 46 consumes relatively little power. In contrast, the conventional registered DRAM modules 10a-c shown in Figures 1 and 2 continues to consume a significant amount of power even if neither of the DRAM devices 12, 14 in the module 10 has been selected. More specifically, the registers 20 used in the modules 10a-c consume power each time signals are latched into the registers 20 responsive to each leading edge of the clock signal. However, the flip-flops 110j-100n that receive the chip select signals CS0#-CS3# are always enabled.

Another embodiment of a register 120 that may be used in the modules 44, 46 is shown in Figure 5. The register 120 again includes a flip-flop 124 for each of the signals that is applied to the register 120. Each flip-flop 124 includes a data "D" input to which the externally applied signal is coupled and a clock input "C" to which the ICLK signal is coupled. Unlike the flip-flops 110 shown in Figure 4, the flip-flops 124 do not include a clock enable "CE" input. Instead an enable signal is generated by an AND gate 130 and is used to control OR gates 134 through which most of the input signals are coupled to the D inputs of respective flip-flops 124. However, the four chip select signals CS0#-CS3# are applied directly to their respective flip-flops 124k-124n without passing through respective NOR gates 134. The chip select signals CS0#-CS3# are also applied to respective inputs of the AND gate 130.

In operation, the output of the AND gate 130 will be low to enable the OR gates 134 if any of the chip select signals CS0#-CS3# is active low. Thus, the register 120 will latch the signals applied to its inputs responsive to the ICLK signal

from the PLL 104 if any of the SDRAMs 90-96 in the module 44, 46 is selected by the memory controller 80. If none of the chip select signals CS0#-CS3# is active low, all of the inputs to the AND gate 130 will be high, thereby causing the AND gate 130 to apply a high to the OR gates 130. The OR gates 130 are then disabled from coupling the input signals to the D inputs of the flip-flops 124. As a result, the non-enabled register in the modules 44, 46 consumes relatively little power if none of the SDRAMs 90-96 in the modules 44, 46 is selected.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. For example, although the register 108 of Figure 4 and the register 120 of Figure 5 include a NAND gate 114 and an AND gate 130, respectively, it will be understood that other logic devices can be alternatively used to decode the chip select signals. Other modifications will be apparent to one skilled in the art. For example, rather than coupling the input signals through an OR gate 134 in the embodiment of Figure 4, the input signals could be applied directly to the D terminals of the flip-flops 124, and the ICLK signal could instead be coupled to the flip-flops 124 through one of the OR gate 134. Accordingly, the invention is not limited except as by the appended claims.